IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: NEMAZIE et al	Art Unit: 2181
Appl. No.: 10/775,523	Examiner: Lee, Chun
Filed: 02/09/2004	Atty. Docket: Siliconstor-0003US
For: Route Aware Serial Advanced Technology Attachment (SATA) Switch	

Appeal Brief Under 37 CFR § 41.37

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Final Office Action mailed August 10 2007, Appellants submit this appeal brief under 37 CFR § 41.37.

The requisite fee of $500 under 37 CFR § 40 (B)(2) and any fees required under 37 CFR. 1. 136(a) for any extension of time required to submit this appeal brief, is sought to be submitted accompanying the filing of this appeal brief. However, the USPTO is directed to charge all required fees (except for the issue fees and the publication fees) to process the pending appeal and credit any overpayments to Deposit Account No. 501638.

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I. REAL PARTY IN INTEREST

This application is assigned to LSI Logic Corporation, by Virtue of the assignment recorded on 10/05/2007, at reel/frame 019927/0098.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

A. Pending Claims

Claims 1-20 are pending. Of these, claims 1, 9, 14, and 19 are independent claims.

B. Rejections

All claims 1-20 were rejected.

In particular, claims 1-7 and 9-20 were rejected under 35 USC § 103(a) as being unpatentable over US Patent Number 6,961,813 issued to Grieff et al (hereinafter "Grieff") in view of U.S. Publication No. 2003/0131166 A1 (hereinafter "Utsunomiya").

Claim 8 was rejected under 35 USC § 103(a) as being unpatentable over Grieff in view of Utsunomiya and further in view of US Patent Number 4,891,788 issued to Kreifels et al (hereinafter "Kreifels").

C. Appealed Claims

All the pending claims 1-20 are subject of this appeal.

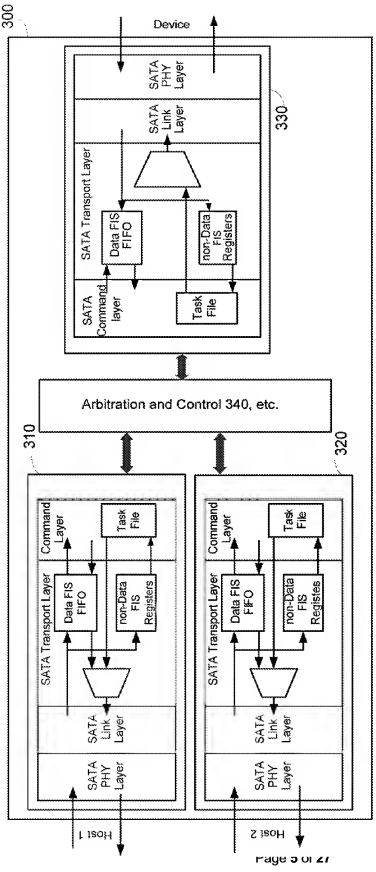
IV. STATUS OF AMENDMENTS

An amendment was filed on October 5, 2007, subsequent to the outstanding final rejection. This amendment was entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed subject matter relates to enabling multiple hosts to concurrently access a single storage device using industry-standard Serial Advanced Technology Attachment (SATA) interface protocol.

By way of convenience, an exemplary embodiment of the present invention is illustrated in the figure below, which is a condensed representation of Fig. 6 from the patent application.


300
Device
SATA PHY Layer
SATA Link Layer
330
SATA Transport Layer
Data FIS FIFO
non-Data FIS Registers
SATA Command layer
Task File
Arbitration and Control 340, etc.
310
320
Command Layer
Task File
SATA Transport Layer
Data FIS FIFO
non-Data FIS Registes
SATA Link Layer
SATA PHY Layer
Host 1
Host 2

In general, the switch 300 includes SATA ports 310 and 320, which are coupled to hosts 1 and 2, respectively. The switch 300 further includes SATA port 330, which is coupled to a Device. The Device is generally a storage device. The features of the various embodiments of the present invention allow the hosts concurrent access to the Device. Concurrency, as used herein, indicates acceptance of commands, from either of two or more hosts, at any given time including when the Device (such as a storage unit) is not in an idle state.

Turning now to the claimed subject matter, claim 1 is directed towards "a switch coupled between a plurality of host units." Claim 1 recites in part "an arbitration and control circuit for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting non-data FIS (frame information structure), from either of the first or second host units, at any given time, including when the device is not in an idle state…"

Thus, the hosts can concurrently access the Device, because the arbitration and control circuit allows the switch to accept non-data FIS from either host at any given time. As recited in claim 1, this is accomplished by using:

> a. a first SATA port including a first host task file responsive to a non-data FIS structure from a first host unit;
>
> b. a second SATA port including a second host task file, responsive to a non-data FIS from a second host unit;

Thus, various embodiments of the present invention innovatively teach using a host task file in each SATA port. It is noted that the first and second task files are located before the arbitration and control circuit therefore allowing concurrent acceptance of commands from the hosts.

Claim 1 further recites "the non-data FIS of the … host units and the device identify which one of the … host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch."

Figure 12 of the instant specification show how, by using reserved bits in the FIS, the FIS organization can be modified to identify the host originating the FIS, making routing of the FIS transparent to the switch.

Claim 2 further defines the storage unit in claim 1. Thus, claim 2 recites "said device is a storage unit."

Claim 3 further defines where the switch in claim 1 is employed. Thus, claim 3 recites "said switch is employed in an enterprise system."

Claim 4 further defines the function of the arbitration and control circuit in claim 1. Thus, claim 4 recites "said arbitration and control circuit causes concurrent access of the device by the first and second host units."

Claim 5 further defines the method used to identify the originating host units in claim 1. Thus, claim 5 recites "a bit is used to indicate which host is the origin or destination of the non-data FIS."

Claim 6 further defines the SATA layer used in the switch in claim 1. Thus, claim 6 recites "said first, second, and third ports are layer 2 ports."

Claim 7 further defines the function provided by the switch in claim 1. Thus, claim 7 recites "the switch provides for 'route aware' routing." The instant application defines route aware routing to be when "the device identifies which one of the hosts is an origin and/or destination so that routing of FIS is transparent to the switch."

Claim 8 further defines the components of the switch in claim 1. Thus, claim 7 recites "the switch further includes a dual ported first-in-first-out (FIFO)."

Claim 9 recites a first and second SATA port, each including a host task file for connection to a first and second host unit respectively, each port responsive to a non-data FIS from the respective host unit. Claim 9 further recites an arbitration and control unit for selecting either the first or second host unit to concurrently access the device, at any time, including when the Device is not in an idle state. Also, Claim 9 recites "wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends non-data FIS to the switch for routing to the device."

Claim 10 further defines the function provided by the switch in Claim 9. Thus, claim 10 recites "the switch provides for 'route aware' routing."

Claim 11 further defines the device used with the switch in Claim 9. Thus, claim 11 recites "said device is a storage unit."

Claim 12 further defines where the switch in claim 9 is employed. Thus, claim 12 recites "said switch is employed in an enterprise system."

Claim 13 further defines the function of the arbitration and control circuit in claim 9. Thus, claim 13 recites "said arbitration and control circuit causes concurrent access of the device by the first and second host units."

Claim 14 is directed towards "a switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (ATA) links, for routing frame information between the first and second host units and the device."

Claim 14 recites in part:

> a. a first serial ATA port, including a first host task file for connection to a first host unit, said first SATA port responsive to a non-data frame information structure (FIS) from the first host unit;
>
> b. a second serial ATA port, including a second host task file for connection to a second host unit, responsive to a non-data FIS from the second host unit

Claim 14 further recites "wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch."

Claim 15 further defines the switch in claim 14. Thus, claim 15 recites "the switch is a serial ATA switch."

Claim 16 further defines the Device used with the switch in claim 14. Thus, claim 16 recites "said device is a storage unit."

Claim 17 further defines where the switch in claim 14 is employed. Thus, claim 17 recites "said switch is employed in an enterprise system."

Claim 18 further defines the function of the arbitration and control circuit in claim 14. Thus, claim 18 recites "said arbitration and control circuit causes concurrent access of the device by the first and second host units."

Claim 19 is directed towards "a method for communication between multiple host units and a device, through a serial advanced technology attachment (ATA) switch coupled to multiple host units and the device using serial ATA links."

Claim 19 recites in part:

e. selecting one of the first or second host units for coupling to the device through the switch when either of the first or second host units sends commands for execution by the device;

f. coupling the device to the selected one of the first or second host units; and

g. while the selected one of the first or second host units is coupled to the device, the other one of the first or second host units sending non-data FIS to the switch for routing to the device

Claim 19 further recites "the non-data FIS of the first and second host units and the device identifying which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch"

Claim 20 further defines the method in claim 19. Thus, claim 20 recites "the steps of transmitting a non-data FIS through the first serial ATA port, non-data FIS through the second serial ATA port, and transmitting a non-data FIS through the third serial ATA port."

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether the rejection of claims 1-7 and 9-20 under 35 USC § 103(a) as being unpatentable over Grieff in view of Utsunomiya is proper.

Whether the rejection of claim 8 was rejected under 35 USC § 103(a) as being unpatentable over Grieff in view of Utsunomiya and further in view of Kreifels is proper.

VII. THE ARGUMENT

A. Brief Introduction to references cited by the examiner

As noted above, claims 1-7 and 9-20 were rejected under 35 USC § 103(a) as being unpatentable over Grieff in view of Utsunomiya, and claim 8 was rejected under 35 USC § 103(a) as being unpatentable over Grieff in view of Utsunomiya and further in view of Kreifels.

A brief introduction to Grieff, Utsunomiya, and Kreifels is now provided.

1. Brief Introduction to *Grieff*

Grieff relates generally to a dual port adapter (DPA) for providing multi-initiator capability to a SATA drive. Grieff uses link-layer (or layer 2) ports on the host and device sides. The host-side ports are specifically described to be state machines. Grieff: Col. 5, lines 50-56. In Grieff, an arbiter connected directly to the host ports arbitrates between the two hosts on a round-robin scheme. Id. The host that wins arbitration is granted access. Thus, under Grieff, only one host is granted access to the device at any given time.

Once a host wins arbitration, commands issued by that host are routed through a mux and to an inbound decoder. Grieff Col. 5, lines 25-30. In the architecture proposed by Grieff, a host is not granted access, and cannot issue commands, until it has won arbitration.

In short, Grieff describes a DPA that uses layer-2 state machine ports to connect to multiple hosts. The DPA arbitrates between the two hosts, meaning only one host can communicate with the DPA at any given time.

2. Brief Introduction to *Utsunomiya*

Utsunomiya relates to a single host and single device system using the older ATA (retroactively renamed parallel ATA or "PATA") interface. Unlike the small computer system interface (SCSI), PATA does not support command queuing, which means that a CPU or host must issue commands one at a time. [See: Utsunomiya, ¶[0004]]. Utsunomiya addresses this limitation by using a task file queue, stored either in the main memory or a host bus adapter

(HBA). [Utsunomiya ¶[0020]]. Utsunomiya deals solely with a PATA interface, therefore the task file queue described in Utsunomiya conforms to the PATA protocol not the SATA protocol.

3. Brief Introduction to *Kreifels*

Kreifels relates to a FIFO with an almost-full and almost-empty flag.

FIFOs are sometimes realized with a dual port RAM cell with a plurality of addressable locations, and read and write pointers that are incremented with each read and write operation, respectively. Full and empty flags prevent users from writing to a full FIFO or reading from an empty FIFO, both of which can result in the read and write pointers to point to the same location.

A half-full flag was also implemented in some FIFOs. Kreifels addresses certain timing problems associated with the half-full flag.

Thus, Kreifels is, in essence, a FIFO.

B. Factual and legal discussions

1. The combination of references do not disclose, suggest, hint at or teach the recited "arbitration and control circuit"

The claimed invention recites "the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch." Claims 1, 9, 14, and 19. However, the combination of references do not disclose an apparatus/method for making the routing of non-data FIS transparent to the switch.

The Office Action dated August 10, 2007 erroneously states, on page 10, paragraph 15, that:

> Grieff further teaches said switch comprising wherein a bit is used to indicate which host is the origin or destination of the non data FIS (Grieff, Col. 4, ll. 47-57 and col. 10, l. 27 to col. 12, l. 29) as each non-data FIS comprise an associated 5-bit tag utilized for identifying which host is the origin or destination of the FIS.

Elsewhere, on page 11, paragraph 17, the office action erroneously states that:

> Grieff further teaches said switch comprising wherein the switch provides for 'route aware' routing (Grieff, col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34; col. 5, l. 17 to col. 6, l. 56 and col. 12, l. 60 to col. 14, l. 21)

The rejection points to several different portions of Grieff. Each is discussed separately hereinbelow.

1- Grieff, Col. 2, l 53 to Col. 3, l 45: This portion of Grieff merely provides an overview of its functionality. But there is no discussion of 'route aware' routing.

2- Grieff, Col. 4, ll 5 to 34: This portion of Grieff provides a background of the differences between SCSI, PATA and SATA in multi-host environments. There is no discussion of 'route aware' routing.

3- Grieff, Col. 4 ll 47-57: It is Applicants' understanding that this citation misconstrues Grieff. These cited discussions relate to "an ATA device that supports command queuing (of certain) commands." (Grieff, ll.47-48). Command queuing is an optional functionality of SATA, as discussed in SATA Rev 2.6 specs, "13.5 Native Command Queuing (Optional)." SATA devices offering this optional SATA feature can queue up to 32 commands internally. [Id.]

Grieff apparently supports the SATA Queued Command feature. [See: Grieff Col. 4, ll. 38-40]. In Grieff, a host "issuing a queued command…places a unique Tag in bits 7-3 of the ATA Sector Count register." [See: Grieff, Col. 4, ll. 53-55]. This "5-bit tag assigned from the host (serves) to uniquely identify a specific command completion when the device completes queued commands out of order." [See: Grieff Col. 4, ll 51-53]. But the Final Office Action of August 10, 2007, erroneously states that the "associated 5-bit tag (is) utilized for identifying which host is the origin or destination of the FIS." Final Office Action of August 10, 2007, page 10, paragraph 15.

Therefore, although this 5-bit tag is used to identify up to 32 queued commands, the Final Office Action erroneously concludes that it is used to identify the host.

4- Grieff, Col. 5, l 17 to Col. 6, l 56: This portion of Grieff actually shows that the claimed invention is absent in Grieff. Specifically, col. 5 l. 67- col. 6 l. 3 recites "In an exemplary embodiment, OR_Table 116 includes a data table that stores the original Tag associated with each outstanding command, the originating source of each outstanding command (i.e. Host 0 or Host 1)…"

Thus, in Grieff, identification of the originating host is done through the OR_Table, which stores Tags tracking the originating host. In contrast, in the claimed invention, the routing is invisible to the switch.

5- Grieff, Col. 10, l. 27 to col. 12, l. 29: These discussions actually show the claimed invention is *absent* in Grieff. The claimed invention uses "non-data FIS…(to) identify which…host unit is an origin and/or destination host so that routing of non-data FIS is transparent to the switch." (claims 1, 9, 14, and 19) In contrast, Grieff uses an Outstanding Request (OR) Table 116, in combination with a Command Tracker State Machine (SM) 114 to route the non-data FIS to the appropriate host.

In Grieff, "When the Command Tracker detects an incoming queued command from the host side interface of the dual port adapter, a new Tag is assigned to the command to guarantee uniqueness of Tags between multiple initiator commands." Grieff, Col. 10, ll 18-31. "The information stored in the OR_Table may include…the host that sent the command." Grieff, Col. 10 ll. 42-46. The "In an exemplary embodiment, OR_Table 116 includes a data table that stores…the originating source of each outstanding command" Grieff Col. 5 l. 67 to Col.6 l. 4. "The Command Tracker SM takes measure to determine the correct host to reconnect to if the D_Status[SERV] bit is set." Grieff, Col. 11, ll 54-56.

6- Grieff, Col. 12, l. 60 to Col. 14, l. 21: This portion of Grieff elaborates on Bus Reconnection Procedures. It does not deal with routing non-data FIS.

In short, whereas the claimed invention uses the non-data FIS itself "so that routing of non-data FIS is transparent to the switch" (claims 1, 9, 14, 19) Grieff assigns a Tag to the commands. The Tags are stored in an OR_Table and tracked by the Command Tracker SM in order to match commands with the issuing host for routing purposes.

Therefore, since Grieff does not include 'route aware' routing, and since the issue of routing FIS among multiple hosts has no relevance to either Utsunomiya or Kreifels, none of the cited references have any methodology to make the routing of non-data FIS transparent to the switch.

Appellants thus submit that the cited combination lacks an element of the claimed invention, and that any combination will not work without re-engineering the art beyond recognition.

2. The claimed invention is not obvious because the proposed combination of references simply does not work

The Office Action of August 10, 2007 states that "it would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Utsunomiya's task file queue (TFQ) into Grieff's ATA ports for the benefit of decreasing the work load of the host unit for issuing commands." Office Action of August 10, 2007, page 8.

In fact, the combination does not work.

The host ports 130 and 132 in Grieff are state machines for relaying primitives with no mention of storage capability. [See: Grieff: Col. 5, lines 50-56]. Indeed, if the capability existed in Grieff's host ports 130 and 132 to store commands or non-data FIS, arguably Grieff would not have needed to store and decode host commands after the switch, i.e. FIS buffer 120.

Furthermore, the host ports 130 and 132 in Grieff operate at the Link Layer (layer 2). In comparison, the TFQs from Utsunomiya function in PATA protocol, which is basically an Application Layer.

By way of brief background, SATA is generally a 4-layer protocol, comprising a physical layer, a link layer (or layer 2), a transport layer, and an application layer (or layer 4). In SATA, the basic unit of communication or exchange is a frame. A frame comprises of a start of frame (SOF) primitive, a frame information structure (FIS), a Cyclic Redundancy Checksum (CRC) and an end of frame (EOF) primitive.

Thus, SATA uses a multi-layer communication protocol with four layers, each with different functionality. [See: SATA Specification ver. 2.6 (February 15, 2007) 42-43]. To properly interact, components must operate on the same layer: a component operating on the link layer (or layer 2) cannot operate on the command layer (layer 4). [See: SATA Specification ver. 2.6 (February 15, 2007) 42-43]. It is noted that command layer and application layer refer to the same layer.

Thus, the link layer host ports 130 and 132 of Grieff, lacking storage capability, can neither store nor interface with the application layer TFQs from Utsunomiya.

Furthermore, the arbiter module 112 of Grieff processes at the Link Layer (layer 2) rather than the command layer (layer 4). [See: Grieff, Col. 5, Lns. 50-56]. Redesigning the arbiter

module 112 would in turn require re-engineering each subsequent component to interact with command layer (layer 4) at the host ports 130, 132. Without redesigning each subsequent component the system simply would not work.

In short, simply "including" Utsunomiya's TFQs into Grieff's ATA ports will not work because at least the following sub-systems will need to be re-engineered or eliminated:

- The ports 130, 132 in Grieff. As recited, these ports don't have storage capability to handle TFQs.

- Utsunomiya's TFQ 22. As recited, the TFQ 22 is "done in software" and resides in RAM 16. Furthermore, it functions in PATA, and is not compatible with SATA FIS.

- Grieff's OR Table 116. If routing of non-data FIS were transparent to the switch, much of the functionality of this sub-system would be rendered useless, but it's unclear that the OR Table could simply be removed.

- Grieff's decoder 120. Much of the functionality of this sub-system would be rendered useless by the TFQs, but it's unclear that the decoder could simply be removed.

- Grieff's decoder command tracker SM 114. This state machine accepts and generates control signals for numerous sub-systems that have to be re-engineered or eliminated. Therefore, Figs. 2 through 8 in Grieff, showing the various states in the command tracker state machine 114, would have to be substantially re-engineered.

The standard for obviousness analysis is set forth in KSR International Co. v. Teleflex Inc., 127 S. Ct. 1727 (2007). In KSR, the Court held that "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art…Inventions in most, if not all, instances rely upon building blocks long since uncovered and claimed discoveries almost of necessity will be combinations of what . . . is already known." Id at 1741.

In analyzing obviousness the Court further held that an invention is obvious where "a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." (emphasis added) Id. at 1742. Here, the combination of elements from Grieff and Utsunomiya cannot simply be put together like a puzzle to yield the claimed invention.

That is, for the foregoing reasons, among others, the TFQs of Utsunomiya *cannot* simply be inserted into the host ports of Grieff.

Any combination of these elements would require, if can be done at all, re-engineering to such an extent as to render them practically unrecognizable.

Appellants thus submit that the cited combination lacks an element of the claimed invention, and that any combination will not work without re-engineering the art beyond recognition.

3. The claimed invention is not obvious because the combination does not disclose, suggest, hint at or teach "selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time"

Because the combination of references does not work, it necessarily lacks the foregoing concurrency limitation.

Appellants thus submit that the cited combination lacks an element of the claimed invention, and that any combination will not work without re-engineering the art beyond recognition.

4. The examiner improperly used hindsight in his finding of obviousness

When the Board does not explain the motivation suggestion or teaching that would have led the skilled artisan at the time of the invention to the claimed combination as a whole, an inference is created that hindsight was used to find obviousness. In re Kahn, 441 F.3d 977, 986.

Here, the Examiner has failed to meet this requirement. Thus, an inference of hindsight is created. The use of hindsight to reject an application as obvious is impermissible. KSR, supra at 1742.

Appellants further submit that improper hindsight was used in the obviousness rejection, and that a *prima facie* case for obviousness has not been made.

5. A prima facie case of obviousness has not been established Because the Examiner has not considered the level of ordinary skill in the pertinent art, or stated a motivation to combine the cited references

In re Kahn, 441 F.3d 977 (Fed. Cir. 2006) sets forth the requirement for a *prima facie* showing of obviousness. Under Kahn, a *prima facie* case is made where "both the scope and content of the prior art and [the] level of ordinary skill in the pertinent art" are considered. *Id.* at 986. Furthermore, in rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to explain the reason(s) why one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious. This entails consideration of both the "scope and content of the prior art" and "level of ordinary skill in the pertinent art." In re Kahn, 441 F.3d 977, 986, cited by the Supreme Court in KSR International v. Teleflex 127 S. Ct. 1727, 1740.

The Examiner cannot simply reach conclusions based on the examiner's own understanding or experience – or on his or her assessment of what would be basic knowledge or common sense. Rather, the Examiner must point to some concrete evidence in the record in support of these findings. In re Zurko, 258 F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 200 1). Thus the Examiner must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the Examiner's conclusion. These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. [See: In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)].

We respectfully submit that the Examiner has clearly not met this burden.

In fact, nothing in Grieff teaches, suggests, or hints at including a task file queue or a FIFO in the host ports. To do so not only requires hindsight, but would also require at least re-designing practically all of Grieff, if it would work at all. It would also require re-designing the TFQ of Utsunomiya.

In particular, in rejecting Claim 1, the Examiner has failed to describe the level of ordinary skill in the pertinent art. Furthermore, the Examiner finds the mere awareness of a task

file queue as sufficient motivation to extend the disclosures of Utsunomiya into Grieff to provide the features in the claimed invention.

Independent claims 9, 14 and 19 each, at least substantially parallel, claim 1 and are thus believed to be allowable for, inter alia, the foregoing reasons with respect to claim 1.

Claims 2, 3, 4, 5, 6, 7, and 8 are also allowable at least as depending from the allowable base claim 1.

Claims 10, 11, 12 and 13 are also allowable at least as depending from the allowable base claim 9.

Claims 15, 16, 17, and 18 are also allowable at least as depending from the allowable base claim 14.

Claim 20 is also allowable at least as depending from the allowable base claim 19.

Additionally, in rejecting Claim 8, the Examiner finds the mere awareness of a FIFO as sufficient motivation to extend the disclosures of Kreifels into Grieff to provide the features in the claimed invention.

C. Conclusion

Appellants thus submit that the combination art of record fails to establish proper rejections. Appellants therefore respectfully request the reversal of all the rejections under 35 U.S.C. § 103, at least for the reasons noted above.

Respectfully submitted,
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VIII. LISTING OF CLAIMS

Claim 1 (previously presented): A switch coupled between a plurality of host units and a device for routing frame information therebetween and comprising:

a. a first serial advanced technology attachment (ATA) port including a first host task file responsive to a non-data frame information structure (FIS) from a first host unit;

b. a second serial ATA port including a second host task file, responsive to a non-data FIS from a second host unit;

c. a third serial ATA port, responsive to a non-data FIS from a device; and

d. an arbitration and control circuit for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state and whenever either one of the first or second host units sends non-data FIS to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive.

Claim 2 (original): A switch as recited in claim 1 wherein said device is a storage unit.

Claim 3 (original): A switch as recited in claim 1 wherein said switch is employed in an enterprise system.

Claim 4 (original): A switch as recited in claim 1 wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units.

Claim 5 (previously presented): A switch as recited in claim 1 wherein a bit is used to indicate which host is the origin or destination of the non-data FIS.

Claim 6 (original): A switch as recited in claim 1 wherein said first, second and third ports are layer 2 ports.

Claim 7 (original): A switch as recited in claim 1 wherein the switch provides for 'route aware' routing.

Claim 8 (previously presented): A switch as recited in claim 1 wherein the switch further includes a dual ported first-in-first-out (FIFO).

Claim 9 (currently amended): A switch comprising:

a. a first serial advanced technology attachment (ATA) port including a first host task file for connection to a first host unit, said first ATA port responsive to a non-data frame information structure (FIS) from the first host unit;
b. a second serial ATA port including a second host task file for connection to a second host unit responsive to a non-data FIS from the second host unit;
c. a third serial ATA port, responsive to a non-data FIS, for connection to a device, the switch for routing frame information between the first and second host units and the device; and

d. an arbitration and control circuit for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state, when either one of the first or second host units sends non-data FIS to the device,

wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends non-data FIS to the switch for routing to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive.

Claim 10 (previously presented): A switch as recited in claim 9 wherein the switch provides for 'route aware' routing.

Claim 11 (original): A switch as recited in claim 9 wherein said device is a storage unit.

Claim 12 (original): A switch as recited in claim 9 wherein said switch is employed in an enterprise system.

Claim 13 (original): A switch as recited in claim 9 wherein said arbitration and control causes concurrent access of the device by the first and second host units.

Claim 14 (currently amended): A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (ATA) links, for routing frame information between the first and second host units and the device, said switch comprising:

a. a first serial ATA port, including a first host task file for connection to a first host unit, said first SATA port responsive to a non-data frame information structure (FIS) from the first host unit;
b. a second serial ATA port, including a second host task file for connection to a second host unit, responsive to a non-data FIS from the second host unit;
c. a third serial ATA port, responsive to a non-data FIS, for connection to a device;
d. an arbitration and control circuit for selecting one of the first or second host units to concurrently access the device through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state, when either the first or second host units sends non-data FIS to the device,

wherein while one of the first or second host units is coupled to the device, the other one of to the first or second host units sends non-data FIS to the switch for routing to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive.

Claim 15 (original): A switch as recited in claim 14 wherein the switch is a serial ATA switch.

Claim 16 (original): A switch as recited in claim 14 wherein said device is a storage unit.

Claim 17 (original): A switch as recited in claim 14 wherein said switch is employed in an enterprise system.

Claim 18 (original): A switch as recited in claim 14 wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units.

Claim 19 (currently amended): A method for communication between multiple host units and a device, through a serial advanced technology attachment (ATA) switch coupled to the multiple host units and the device using serial ATA links routing frame information therebetween comprising:

a. receiving a non-data frame information structure (FIS) through a first serial ATA port, from a first host unit;
b. receiving a non-data FIS, through a second serial ATA port, from a second host unit;
c. receiving a non-data FIS through a third serial ATA port;
d. arbitrating between the first and second host units and the device;
e. selecting one of the first or second host units for coupling to the device through the switch when either of the first or second host units sends commands for execution by the device;
f. coupling the device to the selected one of the first or second host units; and
g. while the selected one of the first or second host units is coupled to the device, the other one of the first or second host units sending non-data FIS to the switch for routing to the device

during the sending step g., the non-data FIS of the first and second host units and the device identifying which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby

reducing the complexity of the design of the switch rendering its manufacturing less expensive.

Claim 20 (previously amended): A method for communication, as recited in claim 19, further including the steps of transmitting a non-data FIS through the first serial ATA port, non-data FIS through the second serial ATA port, and transmitting a non-data FIS through the third serial ATA port.

IX. APPENDIX

A. EVIDENCE APPENDIX: None
B. RELATED PROCEEDINGS APPENDIX: None